IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: M. Okazaki et al.   : Art Unit:
Serial No.:   To Be Assigned   : Examiner:
Filed: Herewith   :
FOR: BUFFER MEMORY ADDRESS TRANSLATION   :
              DEVICE, SECTOR ADDRESS INFORMATION
              RELIABILITY DETERMINATION DEVICE,
              DEFECTIVE SECTOR DETERMINATION DEVICE,
              ECC BLOCK SYNCHRONIZATION DETECTION
              DEVICE, OPTICAL DISK DRIVE, MEDIUM, AND
              PROGRAM

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

S I R :

   Prior to examination, please amend the above application as follows:

IN THE SPECIFICATION:

   After the title and before the first paragraph, please insert the following paragraph:

   THIS APPLICATION IS A U.S. NATIONAL PHASE APPLICATION OF PCT INTERNATIONAL APPLICATION PCT/JP01/04763.

   Please replace the section beginning at page 5, line 15:

   To solve the problems described above, one aspect of the present invention is a buffer memory address translation device, characterized in that the buffer memory address translation device comprises:

   Please replace the paragraph beginning at page 6, line 6:

Another aspect of the present invention is the buffer memory address translation device, characterized in that said positional data is sector address information.

Please replace the paragraph beginning at page 6, line 11:

Still another aspect of the present invention is the buffer memory address translation device, characterized in that said positional data is a frame synchronization code.

Please replace the section beginning at page 6, line 16:

Yet still another aspect of the present invention is the buffer memory address translation device, characterized in that said analysis means comprises:

Please replace the section beginning at page 7, line 14:

Still yet another aspect of the present invention is the buffer memory address translation device, characterized in that said read sector address information has an error detection code added thereto, and

Please replace the paragraph beginning at page 7, line 22:

A further aspect of the present invention is the buffer memory address translation device, characterized in that said determination of reliability is accomplished by determining continuity between said read sector address information and sector address information previously read.

Please replace the section beginning at page 8, line 4:

A still further aspect of the present invention is the buffer memory address translation device, characterized in that said predetermined criterion is a criterion of reliability required by external control means, and

Please replace the section beginning at page 8, line 15:

A yet further aspect of the present invention is a buffer memory address translation device, characterized in that the buffer memory address translation

device comprises:

Please replace the section beginning at page 10, line 3:

A still yet further aspect of the present invention is a sector address information reliability determination device, characterized in that the sector address information reliability determination device comprises:

Please replace the section beginning at page 10, line 24:

An additional aspect of the present invention is a defective sector determination device, characterized in that the defective sector determination device comprises:

Please replace the section beginning at page 11, line 15:

A still additional aspect of the present invention is the defective sector determination device, characterized in that said defective sector detection means detects the number of said defective sectors and the sector physical address information of a leading one of said defective sectors, and

Please replace the section beginning at page 12, line 1:

A yet additional aspect of the present invention is the defective sector determination device, characterized in that said continuity determination means comprises:

Please replace the section beginning at page 12, line 24:

A still yet additional aspect of the present invention is the defective sector determination device, characterized in that said continuity determination means comprises:

Please replace the paragraph beginning at page 13, line 22:

A supplementary aspect of the present invention is the defective sector determination device, characterized in that said position where a difference occurs is a position where there are one or more sectors for which the sector physical

address information is determined to be continuous between two continuous sectors corresponding to the sector address information for which said sector address information is determined to be continuous.

Please replace the paragraph beginning at page 14, line 7:

A still supplementary aspect of the present invention is the defective sector determination device, characterized in that said defective sector detection means regards the sector physical address information of the sector for which said sector logical address information is not continuous as the sector physical address information of said leading one of the defective sectors.

Please replace the paragraph beginning at page 14, line 16:

A yet supplementary aspect of the present invention is the defective sector determination device, characterized in that said defective sector detection means detects the number of sectors for which said sector physical address information is determined to be continuous and that exist between the two sectors corresponding to the sector logical address information determined to be continuous, and regards said number of detected sectors as said number of defective sectors.

Please replace the section beginning at page 15, line 1:

A still yet supplementary aspect of the present invention is an ECC block synchronization detection device, characterized in that the ECC block synchronization device comprises:

Please replace the section beginning at page 15, line 22:

Another aspect of the present invention is an optical disk drive, characterized in that the optical disk drive comprises:

Please replace the section beginning at page 16, line 12:

said controller has the buffer address translation device, sector address reliability determination device, defective sector determination device, or ECC block synchronization detection device.

Please replace the section beginning at page 16, line 12:

Still another aspect of the present invention is a medium capable of being processed by a computer, characterized in that the medium stores a program for making the computer serve as whole or part of the analysis means of analyzing a synchronization pattern included in data read from an optical disk medium and positional data allowing a data position to be recognized included in the data read from said optical disk medium, and

Please replace the section beginning at page 16, line 21:

the address generation means of generating an address for storage into a buffer memory based on a result of said analysis of the buffer memory address translation device.

Please replace the section beginning at page 17, line 1:

Yet still another aspect of the present invention is a medium capable of being processed by a computer, characterized in that the medium stores a program for making the computer serve as whole or part of the readout means of reading a frame synchronization code added to data read from an optical disk medium,

Please replace the section beginning at page 18, line 6:

the address generation means of generating an address for storage into a buffer memory based on said frame position found by said frame position interpolation means or the frame position determined by said frame position determination means of the buffer memory address translation device.

Please replace the section beginning at page 18, line 12:

Still yet another aspect of the present invention is a medium capable of being processed by a computer, characterized in that the medium stores a program for making the computer serve as whole or part of the error detection means of detecting an error of sector address information included in data read from an optical disk medium and having an error detection code added thereto,

Please replace the section beginning at page 19, line 1:

the reliability determination means of determining the reliability of said sector address information based on the result of the error detection for said sector address information and the result of the continuity determination for said sector address information with reference to a predetermined condition set by said external control means of the sector address information reliability determination device.

Please replace the section beginning at page 19, line 9:

A further aspect of the present invention is a medium capable of being processed by a computer, characterized in that the medium stores a program for making the computer serve as whole or part of the continuity detection means of detecting a position where a difference occurs between the continuity of said sector physical address information and the continuity of said sector logical address information,

Please replace the section beginning at page 20, line 1:

A still further aspect of the present invention is a medium capable of being processed by a computer, characterized in that the medium storing a program for making the computer serve as whole or part of the error detection means of detecting an error of sector address information that is read from an optical disk medium and has an error correcting code added thereto across n sectors (n = integer) and the error correcting code accommodated in the continuous n sectors,

Please replace the section beginning at page 20, line 15:

the ECC block detection means of, if said sector address information error detection means detects no error in said read sector address information, comparing said quotient of said read sector address information with the previously found quotient and determining that the ECC block synchronization is detected if the comparison does not result in a match of the ECC block synchronization detection device.

Please replace the section beginning at page 20, line 23:

A yet further aspect of the present invention is a program for making the computer serve as whole or part of the analysis means of analyzing a synchronization pattern included in data read from an optical disk medium and positional data allowing a data position to be recognized included in the data read from said optical disk medium, and

Please replace the section beginning at page 21, line 9:

A still yet further aspect of the present invention is a program for making the computer serve as whole or part of the readout means of reading a frame synchronization code added to data read from an optical disk medium,

Please replace the section beginning at page 22, line 13:

the address generation means of generating an address for storage into a buffer memory based on said frame position found by said frame position interpolation means or the frame position determined by said frame position determination means of the buffer memory address translation device.

Please replace the section beginning at page 22, line 19:

An additional aspect of the present invention is a program for making the computer serve as whole or part of the error detection means of detecting an error of sector address information included in data read from an optical disk medium and having an error detection code added thereto,

Please replace the section beginning at page 23, line 7:

the reliability determination means of determining the reliability of said sector address information based on the result of the error detection for said sector address information and the result of the continuity determination for said sector address information with reference to a predetermined condition set by said external control means of the sector address information reliability determination device.

Please replace the section beginning at page 23, line 15:

A still additional aspect of the present invention is a program for making the computer serve as whole or part of the continuity detection means of detecting a position where a difference occurs between the continuity of said sector physical address information and the continuity of said sector logical address information,

Please replace the section beginning at page 23, line 24:

the informing means of informing an external control means of said detected defective sector of the defective sector determination device in readout from a rewritable optical disk medium storing said sector physical address information that is a physical address of said sector besides said sector logical address information included in data.

Please replace the section beginning at page 24, line 6:

A yet additional aspect of the present invention is a program for making the computer serve as whole or part of the error detection means of detecting an error of sector address information that is read from an optical disk medium and has an error correcting code added thereto across n sectors (n = integer) and the error correcting code accommodated in the continuous n sectors,

Please replace the section beginning at page 24, line 19:

the ECC block detection means of, if said sector address information error detection means detects no error in said read sector address information, comparing said quotient of said read sector address information with the previously found quotient and determining that the ECC block synchronization is detected if the comparison does not result in a match of the ECC block synchronization detection device.

Please replace the section beginning at page 29, line 6:

205   High order ID bit address translation decoder

Please replace the section beginning at page 29, line 17:

303   Frame synchronization code encoding block

Please replace the section beginning at page 29, line 19:

305   Sector synchronization detection block

Please replace the section beginning at page 30, line 22:

406   ECC block synchronization signal generation block

Please replace the section beginning at page 31, line 11:

503   Frame position detection decoder

Please replace the section beginning at page 32, line 2:

611   Address component of ID information of ID acquisition signal 411

Please replace the section beginning at page 32, line 4:

612   Error detection result component of ID information of ID acquisition
signal 411

Please replace the paragraph beginning at page 33, line 5:

As an example of the present invention, an optical disk drive is
characterized in that an address used for accurately storing data read from an
optical disk medium into a buffer memory is generated and that even if an
abnormality occurs in various kinds of synchronization indicating a beginning of a
data unit due to various factors such as a fingerprint or scratch on the optical disk
medium, the address used for accurately storing the data read from the optical disk
medium into the buffer memory can be generated by analyzing the data read from
the optical disk medium and grasping a positional relationship between the data
read from the optical disk medium and data previously stored in the buffer
memory.

Please replace the paragraph beginning at page 37, line 18:

As an example of the present invention, the defective sector determination
device is characterized in that it comprises means of reading the physical sector

address information, means of detecting an error in the physical sector address information read by the above means, means of storing the previous physical sector address information of the physical sector address information that is determined to be reliable by the means of detecting an error in the physical sector address information, and means of comparing the stored previous physical sector address information with the current physical sector address information, and determines the continuity of the physical sector address that is determined to be reliable by the means of detecting an error in the physical sector address information.

Please replace the paragraph beginning at page 38, line 8:

As an example of the present invention, the defective sector determination device is characterized in that it comprises means of reading the sector address information, means of detecting an error in the sector address information read by the above means, means of storing the previous sector address information of the sector address information that is determined to be reliable by the means of detecting an error in the sector address information, and means of comparing the stored previous sector address information with the current sector address information, and determines the continuity of the sector address that is determined to be reliable by the means of detecting an error in the sector address information.

Please replace the paragraph beginning at page 47, line 22:

The channel data input to the controller block 107 from the RF signal processing block 104 is first subject to a demodulation processing in the structure shown in Figure 3. That is, Figure 3 shows a structure of demodulation processing means of this embodiment. In Figure 3, reference numeral 301 denotes a channel data parallelization block, reference numeral 302 denotes a frame synchronization signal generation block, reference numeral 303 denotes a frame synchronization code encoding block, reference numeral 304 denotes a data demodulation block, reference numeral 305 denotes a sector synchronization detection block, reference numeral 306 denotes a sector synchronization interpolation block, reference numeral 307 denotes a frame synchronization counter block, reference numeral 308 denotes a frame position detection block, reference numeral 309 denotes a

sector synchronization signal generation block, reference numeral 310 denotes a frame synchronization position reliability determination block, and reference numeral 311 denotes a frame synchronization counter value address translation block.

Please replace the paragraph beginning at page 51, line 20:

Now, an operation of the frame position detection block 308 and frame position reliability determination block 310 will be described in detail with reference to Figure 5. In Figure 5, reference numeral 501 denotes a frame synchronization code encoding register A, reference numeral 502 denotes a frame synchronization code encoding register B, reference numeral 503 denotes a frame position detection decoder, reference numeral 505 denotes a frame synchronization code arrangement OK counter, and reference numeral 506 denotes a frame position detection result adoption determination circuit. Here, the frame position detection block 308 is constituted by the frame synchronization code encoding register A 501, frame synchronization code encoding register B 502, and frame position detection decoder 503, and the frame position reliability determination block 310 is constituted by the frame synchronization code arrangement OK counter 505 and frame position detection result adoption determination circuit 506.

Please replace the paragraph beginning at page 53, line 7:

The frame position decoder 503 takes in values included in the frame synchronization code 324, (n-1)th frame synchronization code signal 511, and (n-2)th frame synchronization code signal 512 for each frame synchronization signal 323. Here, the three values taken in the frame position detection decoder 503 constitute the frame synchronization codes of a current frame, frame one frame ahead of the current frame, and frame two frames ahead of the current frame.

Please replace the paragraph beginning at page 56, line 24:

The count value of the frame synchronization counter block 307 is output to the sector synchronization interpolation block 306 and frame synchronization counter value address translation block 311 as an absolute frame position signal

327.

Please replace the paragraph beginning at page 58, line 28:

The frame synchronization counter value address translation block 331 decodes the absolute frame position signal 327 and generates a frame address 332 that is a base address of the buffer memory for storing the frame.

Please replace the paragraph beginning at page 62, line 14:

The address comparator B 602 compares the high order 20 bits of the address component 611 of the ID information of the ID acquisition signal 411 with the high order 20 bits of the address component of a current ID information signal 417 described later, and outputs a high order address determination result signal 416 to the ECC block synchronization determination block 402 if the comparison does not result in a match. Here, the address component 611 of the ID information of the ID acquisition signal 411 and address component of the current ID information signal 417 described later are two continuous addresses at the timing of the sector synchronization signal 331. In addition, the ECC block of the DVD 101 is constituted by 16 sectors each beginning with the low order four bits of the address represented in the hexadecimal notation included in the ID information of "0000b". Therefore, the high order address determination result signal 416 can be considered to indicate the comparison result of quotients of "(read sector address information) / (number of sectors constituting the ECC block)" of the two continuous sectors, and indicate the change of the ECC block.

Please replace the paragraph beginning at page 63, line 22:

The selector 604 selects the ID acquisition signal 411 if the address reliability OK signal 415 indicates that the ID acquisition signal 411 is reliable, or selects the address expected value signal 618 described later if the address reliability OK signal 415 indicates that the ID acquisition signal 411 is not reliable, and outputs the selected address information as a current address selection signal 619 to the ID retaining register 606.

Please replace the paragraph beginning at page 64, line 10:

The incrementer 605 is a circuit that adds 1 to the value of the current ID information signal 417, and outputs the addition result as the address expected value signal 618 to the selector 604 and address comparator A 601. The reason why the addition result becomes the address expected value signal 616 is that the address component included in the ID information of the DVD 101 has a rule that when the sector is advanced by one, the address component is also advanced by one.

Please replace the paragraph beginning at page 66, line 4:

The ID information address translation block 407 takes in the current ID information signal 417 at each ECC block synchronization signal 418 and generates a sector address 419 and ECC block address 420 that are the base addresses of the buffer memories storing the sector and ECC block, respectively. Here, the sector address 419 must be set to include 26 or more regions for storing the frames, and the ECC block address 420 must be set to include 16 or more regions for storing the sectors.

Please replace the paragraph beginning at page 66, line 13:

Lastly, an eventual generation of a data storage address in the buffer memory 106 will be described with reference to Figure 2. Figure 2 shows a structure of address generation means 1202 of this embodiment. In Figure 2, reference numeral 201 denotes a byte counter, reference numeral 202 denotes a frame synchronization counter value address translation decoder, reference numeral 203 denotes a low order ID address translation decoder, reference numeral 204 denotes an adder/subtracter, reference numeral 205 denotes a high order ID address translation decoder, and reference numeral 206 denotes an adder. In this regard, the frame synchronization counter value address translation block 311 in Figure 3 is equivalent to the frame synchronization counter value address translation decoder 202 in Figure 2, and the ID information address translation block 407 in Figure 4 is constituted by the low order ID address translation decoder 203, adder/subtracter 204, and high order ID address translation decoder 205.

Please replace the paragraph beginning at page 67, line 16:

The frame synchronization counter value address translation decoder 202 is a decoder that takes in the absolute frame position signal 327 at the frame synchronization signal 323 and provides an output shown in Figure 9(a) with respect to the input of the absolute frame position signal 327, and the decoding result is output as the frame address 332 to the adder 206.

Please replace the paragraph beginning at page 67, line 23:

The low order ID address translation decoder 203 is a decoder that takes in the low order four bits of the current ID information signal 417 at the sector synchronization signal 331 and provides an output shown in Figure 9(b) with respect to the input of the low order four bits of the current ID information signal 417, and the decoding result is output as the sector address 419 to the adder 206.

Please replace the paragraph beginning at page 68, line 6:

The adder/subtracter 204 subtracts the high order 20 bits of the ID information 221 corresponding to the data that is preset by the control microcomputer 108 and requested from the host 109 from the high order 20 bits of the current ID information signal 417. In this process, the respective low order four bits thereof are rounded down. Positional information 212 on a start of storage into the buffer memory 106 is added to the calculation result, and the result thereof is output as ECC block position information 214 to the high order ID address translation decoder 205.

Please replace the paragraph beginning at page 69, line 20:

As described above, even if the data read from the DVD 101 cannot be stored in the buffer memory 106, the address of the data storage into the buffer memory 106 is corrected to be normal by detecting an absolute position of the data in each of the data structures by means of the frame position detection block 308, frame position reliability determination block 310, and ID reliability determination block 405, and translating it into an address by means of the frame synchronization counter value address translation decoder 202, low order ID address translation decoder 203, and high order ID address translation decoder 205, and accordingly, an optical disk drive with an enhanced replaying capability

can be constructed.

Please replace the paragraph beginning at page 73, line 20:

As a result, the physical ID retaining register B 1102 stores therein only the physical ID that is reliably free of error, and only the physical ID signal 1114 of the physical ID that is reliably free of error is output to the incrementer A 1103. In addition, the ID retaining register 1105 stores therein only the address component of the ID information that is reliably free of error, and only the ID signal 1117 that is reliably free of error is output to the incrementer B 1106.

Please replace the paragraph beginning at page 75, line 14:

With such a configuration, in replay of a disk having data written thereon according to a defect sector management method for a DVD-RAM of skipping only a defective sector as shown in Figure 10(a) or a disk having data written thereon according to a defect sector management method for a DVD-RAM of skipping an ECC block including a defective sector as shown in Figure 10(b), the presence of a defective sector, the start address of the defective sector, and the number of defective sectors can be detected when the condition that the subtracter 1104 does not exhibit zero is satisfied and the comparator 1107 indicates the continuity of the ID information.

Please replace the paragraph beginning at page 78, line 20:

In addition, the frame synchronization code encoding block 303 of this embodiment is an example of the frame synchronization code readout means of the present invention, the frame synchronization code encoding register A 501 and frame synchronization code encoding register B 502 of this embodiment are an example of the storage means of the present invention, the frame position detection decoder 503 of this embodiment is an example of the continuity determination means of the present invention, the frame synchronization code arrangement OK counter 505 of this embodiment is an example of the counter means of the present invention, the frame position detection result adoption determination circuit 506 of this embodiment is an example of the frame position determination means of the present invention, the frame position determination

condition 513 of this embodiment is an example of the predetermined condition of the present invention, the frame synchronization counter block 307 of this embodiment is an example of the frame position interpolation means of the present invention, and the frame synchronization counter value address translation block 332 of this embodiment is an example of the address generation means of the present invention.

CLAIMS:

Please replace claims 7, 9, and 10 with the following amended claims:

1   7. (As Amended) The buffer memory address translation device according
2   to claim 4, characterized in that said predetermined criterion is a criterion of
3   reliability required by external control means, and

4   said sector address information selection means selects one of the two
5   pieces of the sector address information by analyzing the criterion of reliability
6   required by said external control means and said determination result of said sector
7   address information reliability determination means.

1   9. (As Amended) A sector address information reliability determination
2   device, characterized in that the sector address information reliability
3   determination device comprises:

4   error detection means of detecting an error of sector address information
5   included in data read from an optical disk medium and having an error detection
6   code added thereto;

7   sector address information continuity determination means of comparing
8   said sector address information currently extracted from said read data with said
9   sector address information previously extracted to determine the continuity of said
10   sector address information; and

11   reliability determination means of determining the reliability of said sector
12   address information based on the result of the error detection for said sector
13   address information and the result of the continuity determination for said sector

14   address information with reference to a predetermined condition set by an external
15   control means.

1   10. (As Amended) In readout from a rewritable optical disk medium
2   storing sector physical address information that is a physical address of a sector
3   besides sector logical address information included in data,

4   a defective sector determination device, characterized in that the defective
5   sector determination device comprises:

6   continuity detection means of detecting a position where a difference occurs
7   between the continuity of said sector physical address information and the
8   continuity of said sector logical address information;

9   defective sector detection means of finding a defective sector using said
10   detected difference; and

11   informing means of informing an external control means of said detected

12 defective sector.

Respectfully submitted,

Allan Ratner, Reg. No. 19,717
Attorney for Applicants

AR/dlm/lm

Enclosure: Version With Markings Showing Changes Made
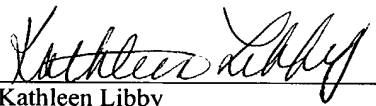
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Kathleen Libby

VERSION WITH MARKINGS SHOWING CHANGES MADE

SPECIFICATION:

After the title and before the first paragraph:

THIS APPLICATION IS A U.S. NATIONAL PHASE APPLICATION OF PCT INTERNATIONAL APPLICATION PCT/JP01/04763.

Specification at page 5, line 15:

To solve the problems described above, ~~the 1st invention~~ one aspect of the present invention ~~(corresponding to claim 1)~~ is a buffer memory address translation device, characterized in that the buffer memory address translation device comprises:

Specification at page 6, line 6:

~~The 2nd invention~~ Another aspect of the present invention ~~(corresponding to claim 2)~~ is the buffer memory address translation device ~~according to the 1st invention~~, characterized in that said positional data is sector address information.

Specification at page 6, line 11:

~~The 3rd invention~~ Still another aspect of the present invention ~~(corresponding to claim 3)~~ is the buffer memory address translation device ~~according to the 1st invention~~, characterized in that said positional data is a frame synchronization code.

Specification at page 6, line 16:

~~The 4th invention~~ Yet still another aspect of the present invention ~~(corresponding to claim 4)~~ is the buffer memory address translation device ~~according to the 2nd invention~~, characterized in that said analysis means comprises:

Specification at page 7, line 14:

~~The 5th invention~~ Still yet another aspect of the present invention ~~(corresponding to claim 5)~~ is the buffer memory address translation device ~~according to the 4th invention~~, characterized in that said read sector address information has an error detection code added thereto, and

Specification at page 7, line 22:

~~The 6th invention~~ A further aspect of the present invention ~~(corresponding to claim 6)~~ is the buffer memory address translation device ~~according to the 4th invention~~, characterized in that said determination of reliability is accomplished by determining continuity between said read sector address information and sector address information previously read.

Specification at page 8, line 4:

~~The 7th invention~~ A still further aspect of the present invention ~~(corresponding to claim 7)~~ is the buffer memory address translation device ~~according to the 4th invention~~, characterized in that said predetermined criterion is a criterion of reliability required by external control means, and

Specification at page 8, line 15:

~~The 8th invention~~ A yet further aspect of the present invention ~~(corresponding to claim 8)~~ is a buffer memory address translation device, characterized in that the buffer memory address translation device comprises:

Specification at page 10, line 3:

~~The 9th invention~~ A still yet further aspect of the present invention ~~(corresponding to claim 9)~~ is a sector address information reliability determination device, characterized in that the sector address information reliability determination device comprises:

Specification at page 10, line 24:

~~The 10th invention~~ An additional aspect of the present invention ~~(corresponding to claim 10)~~ is a defective sector determination device,

characterized in that the defective sector determination device comprises:

Specification at page 11, line 15:

~~The 11th invention~~ A still additional aspect of the present invention ~~(corresponding to claim 11)~~ is the defective sector determination device ~~according to the 10th invention)~~, characterized in that said defective sector detection means detects the number of said defective sectors and the sector physical address information of a leading one of said defective sectors, and

Specification at page 12, line 1:

~~The 12th invention~~ A yet additional aspect of the present invention ~~(corresponding to claim 12)~~ is the defective sector determination device ~~according to the 10th invention~~, characterized in that said continuity determination means comprises:

Specification at page 12, line 24:

~~The 13th invention~~ A still yet additional aspect of the present invention ~~(corresponding to claim 13)~~ is the defective sector determination device ~~according to the 10th invention~~, characterized in that said continuity determination means comprises:

Specification at page 13, line 22:

~~The 14th invention~~ A supplementary aspect of the present invention ~~(corresponding to claim 14)~~ is the defective sector determination device ~~according to the 10th invention~~, characterized in that said position where a difference occurs is a position where there are one or more sectors for which the sector physical address information is determined to be continuous between two continuous sectors corresponding to the sector address information for which said sector address information is determined to be continuous.

Specification at page 14, line 7:

~~The 15th invention~~ A still supplementary aspect of the present invention

(corresponding to claim 15) is the defective sector determination device according to the 11th invention, characterized in that said defective sector detection means regards the sector physical address information of the sector for which said sector logical address information is not continuous as the sector physical address information of said leading one of the defective sectors.

Specification at page 14, line 16:

The 16th invention A yet supplementary aspect of the present invention (corresponding to claim 16) is the defective sector determination device according to the 11th invention, characterized in that said defective sector detection means detects the number of sectors for which said sector physical address information is determined to be continuous and that exist between the two sectors corresponding to the sector logical address information determined to be continuous, and regards said number of detected sectors as said number of defective sectors.

Specification at page 15, line 1:

The 17th invention A still yet supplementary aspect of the present invention (corresponding to claim 17) is an ECC block synchronization detection device, characterized in that the ECC block synchronization device comprises:

Specification at page 15, line 22:

The 18th invention Another aspect of the present invention (corresponding to claim 18) is an optical disk drive, characterized in that the optical disk drive comprises:

Specification at page 16, line 12:

said controller has the buffer address translation device, sector address reliability determination device, defective sector determination device, or ECC block synchronization detection device according to any of claims 1 to 17 implemented therein.

Specification at page 16, line 12:

The 19th invention Still another aspect of the present invention (corresponding to claim 19) is a medium capable of being processed by a computer, characterized in that the medium stores a program for making the computer serve as whole or part of the analysis means of analyzing a synchronization pattern included in data read from an optical disk medium and positional data allowing a data position to be recognized included in the data read from said optical disk medium, and

Specification at page 16, line 21:

the address generation means of generating an address for storage into a buffer memory based on a result of said analysis of the buffer memory address translation device according to the 1st invention.

Specification at page 17, line 1:

The 20th invention Yet still another aspect of the present invention (corresponding to claim 20) is a medium capable of being processed by a computer, characterized in that the medium stores a program for making the computer serve as whole or part of the readout means of reading a frame synchronization code added to data read from an optical disk medium,

Specification at page 18, line 6:

the address generation means of generating an address for storage into a buffer memory based on said frame position found by said frame position interpolation means or the frame position determined by said frame position determination means of the buffer memory address translation device according to the 8th invention.

Specification at page 18, line 12:

The 21st invention Still yet another aspect of the present invention (corresponding to claim 21) is a medium capable of being processed by a computer, characterized in that the medium stores a program for making the computer serve as whole or part of the error detection means of detecting an error of sector address information included in data read from an optical disk medium

and having an error detection code added thereto,

Specification at page 19, line 1:

the reliability determination means of determining the reliability of said sector address information based on the result of the error detection for said sector address information and the result of the continuity determination for said sector address information with reference to a predetermined condition set by said external control means of the sector address information reliability determination device according to the 9th invention.

Specification at page 19, line 9:

The 22nd invention A further aspect of the present invention (corresponding to claim 22) is a medium capable of being processed by a computer, characterized in that the medium stores a program for making the computer serve as whole or part of the continuity detection means of detecting a position where a difference occurs between the continuity of said sector physical address information and the continuity of said sector logical address information,

Specification at page 20, line 1:

The 23rd invention A still further aspect of the present invention (corresponding to claim 23) is a medium capable of being processed by a computer, characterized in that the medium storing a program for making the computer serve as whole or part of the error detection means of detecting an error of sector address information that is read from an optical disk medium and has an error correcting code added thereto across n sectors (n = integer) and the error correcting code accommodated in the continuous n sectors,

Specification at page 20, line 15:

the ECC block detection means of, if said sector address information error detection means detects no error in said read sector address information, comparing said quotient of said read sector address information with the previously found quotient and determining that the ECC block synchronization is detected if the comparison does not result in a match of the ECC block

synchronization detection device ~~according to the 17th invention~~.

Specification at page 20, line 23:

~~The 24th invention~~ A yet further aspect of the present invention ~~(corresponding to claim 24)~~ is a program for making the computer serve as whole or part of the analysis means of analyzing a synchronization pattern included in data read from an optical disk medium and positional data allowing a data position to be recognized included in the data read from said optical disk medium, and

Specification at page 21, line 9:

~~The 25th invention~~ A still yet further aspect of the present invention ~~(corresponding to claim 25)~~ is a program for making the computer serve as whole or part of the readout means of reading a frame synchronization code added to data read from an optical disk medium,

Specification at page 22, line 13:

the address generation means of generating an address for storage into a buffer memory based on said frame position found by said frame position interpolation means or the frame position determined by said frame position determination means of the buffer memory address translation device ~~according to the 8th invention~~.

Specification at page 22, line 19:

~~The 26th invention~~ An additional aspect of the present invention ~~(corresponding to claim 26)~~ is a program for making the computer serve as whole or part of the error detection means of detecting an error of sector address information included in data read from an optical disk medium and having an error detection code added thereto,

Specification at page 23, line 7:

the reliability determination means of determining the reliability of said sector address information based on the result of the error detection for said sector

address information and the result of the continuity determination for said sector address information with reference to a predetermined condition set by said external control means of the sector address information reliability determination device according to the 9th invention.

Specification at page 23, line 15:

The 27th invention A still additional aspect of the present invention (corresponding to claim 27) is a program for making the computer serve as whole or part of the continuity detection means of detecting a position where a difference occurs between the continuity of said sector physical address information and the continuity of said sector logical address information,

Specification at page 23, line 24:

the informing means of informing an external control means of said detected defective sector of the defective sector determination device according to the 10th invention in readout from a rewritable optical disk medium storing said sector physical address information that is a physical address of said sector besides said sector logical address information included in data.

Specification at page 24, line 6:

The 28th invention A yet additional aspect of the present invention (corresponding to claim 28) is a program for making the computer serve as whole or part of the error detection means of detecting an error of sector address information that is read from an optical disk medium and has an error correcting code added thereto across n sectors (n = integer) and the error correcting code accommodated in the continuous n sectors,

Specification at page 24, line 19:

the ECC block detection means of, if said sector address information error detection means detects no error in said read sector address information, comparing said quotient of said read sector address information with the previously found quotient and determining that the ECC block synchronization is detected if the comparison does not result in a match of the ECC block

synchronization detection device ~~according to the 17th invention~~.

Specification at page 29, line 6:

205   ~~ID high order~~ High order ID bit address translation decoder

Specification at page 29, line 17:

303   ~~Data demodulation block~~Frame synchronization code encoding block

Specification at page 29, line 19:

305   ~~Frame synchronization detection block~~Sector synchronization detection block

Specification at page 30, line 22:

406   ECC block synchronization signal generation block

Specification at page 31, line 11:

503   Frame ~~synchronization code~~ position detection decoder

Specification at page 32, line 2:

611   Address component of ID information of ID acquisition signal ~~413~~411

Specification at page 32, line 4:

612   Error detection result component of ID information of ID acquisition signal ~~413~~411

Specification at page 33, line 5:

As an example of the present invention, an optical disk ~~generation device~~ drive is characterized in that an address used for accurately storing data read from an optical disk medium into a buffer memory is generated and that even if an

abnormality occurs in various kinds of synchronization indicating a beginning of a data unit due to various factors such as a fingerprint or scratch on the optical disk medium, the address used for accurately storing the data read from the optical disk medium into the buffer memory can be generated by analyzing the data read from the optical disk medium and grasping a positional relationship between the data read from the optical disk medium and data previously stored in the buffer memory.

Specification at page 37, line 18:

As an example of the present invention, the ~~continuity of the physical sector address information~~defective sector determination device is characterized in that it comprises means of reading the physical sector address information, means of detecting an error in the physical sector address information read by the above means, means of storing the previous physical sector address information of the physical sector address information that is determined to be reliable by the means of detecting an error in the physical sector address information, and means of comparing the stored previous physical sector address information with the current physical sector address information, and determines the continuity of the physical sector address that is determined to be reliable by the means of detecting an error in the physical sector address information.

Specification at page 38, line 8:

As an example of the present invention, the ~~continuity of the sector address information~~defective sector determination device is characterized in that it comprises means of reading the sector address information, means of detecting an error in the sector address information read by the above means, means of storing the previous sector address information of the sector address information that is determined to be reliable by the means of detecting an error in the sector address information, and means of comparing the stored previous sector address information with the current sector address information, and determines the continuity of the sector address that is determined to be reliable by the means of detecting an error in the sector address information.

Specification at page 47, line 22:

The channel data input to the controller block 107 from the RF signal processing block 104 is first subject to a demodulation processing in the structure shown in Figure 3. That is, Figure 3 shows a structure of demodulation processing means of this embodiment. In Figure 3, reference numeral 301 denotes a channel data parallelization block, reference numeral 302 denotes a frame synchronization signal generation block, reference numeral 303 denotes a frame synchronization code encoding block, reference numeral 304 denotes a data demodulation block, reference numeral 305 denotes a sector synchronization detection block, reference numeral 306 denotes a sector synchronization interpolation block, reference numeral 307 denotes a frame synchronization counter block, reference numeral 308 denotes a frame position detection block, reference numeral 309 denotes a sector synchronization signal generation block, reference numeral 310 denotes a frame synchronization position reliability determination block, and reference numeral 311 denotes a frame synchronization counter value address translation block.

Specification at page 51, line 20:

Now, an operation of the frame position detection block 308 and frame position reliability determination block 310 will be described in detail with reference to Figure 5. In Figure 5, reference numeral 501 denotes a frame synchronization code encoding register A, reference numeral 502 denotes a frame synchronization code encoding register B, reference numeral 503 denotes a frame ~~synchronization code~~ position detection decoder, reference numeral 505 denotes a frame synchronization code arrangement OK counter, and reference numeral 506 denotes a frame position detection result adoption determination circuit. Here, the frame position detection block 308 is constituted by the frame synchronization code encoding register A 501, frame synchronization code encoding register B 502, and frame position detection decoder 503, and the frame position reliability determination block 310 is constituted by the frame synchronization code arrangement OK counter 505 and frame position detection result adoption determination circuit 506.

Specification at page 53, line 7:

The frame ~~synchronization~~ position decoder 503 takes in values included in
the frame synchronization code 324, (n-1)th frame synchronization code signal
511, and (n-2)th frame synchronization code signal 512 for each frame
synchronization signal 323. Here, the three values taken in the frame position
detection decoder 503 constitute the frame synchronization codes of a current
frame, frame one frame ahead of the current frame, and frame two frames ahead of
the current frame.

Specification at page 56, line 24:

The count value of the frame synchronization counter block 307 is output to
the sector synchronization interpolation block 306 and frame synchronization
counter value address translation block 311 as an absolute frame position signal
~~326~~327.

Specification at page 58, line 28:

The frame synchronization counter value address translation block 331
decodes the absolute frame ~~synchronization~~ position signal 327 and generates a
frame address 332 that is a base address of the buffer memory for storing the
frame.

Specification at page 62, line 14:

The address comparator B 602 compares the high order 20 bits of the
address component 611 of the ID information of the ID acquisition signal 411 with
the high order 20 bits of the address component of a current ID information signal
417 described later, and outputs a high order address determination result signal
416 to the ECC block synchronization determination block 402 if the comparison
does not result in a match. Here, the address component 611 of the ID information
of the ID acquisition signal 411 and address component of the current ID
information signal 417 described later are two continuous addresses at the timing
of the sector synchronization signal 331. In addition, the ECC block of the DVD
101 is constituted by 16 sectors each beginning with the low order four bits of the
address represented in the hexadecimal notation included in the ID information of
"0000b". Therefore, the high order address determination result signal 416 can be

considered to indicate the comparison result of quotients of "(read sector address information) / (number of sectors constituting the ECC block)" of the two continuous sectors, and indicate the change of the ECC block.

Specification at page 63, line 22:

The selector 604 selects the ID acquisition signal 411 if the address reliability OK signal 415 indicates that the ID acquisition signal 411 is reliable, or selects the address expected value signal ~~616~~618 described later if the address reliability OK signal 415 indicates that the ID acquisition signal 411 is not reliable, and outputs the selected address information as a current address selection signal ~~615~~619 to the ID retaining register 606.

Specification at page 64, line 10:

The incrementer 605 is a circuit that adds 1 to the value of the current ID information signal 417, and outputs the addition result as the address expected value signal ~~616~~618 to the selector 604 and address comparator A 601. The reason why the addition result becomes the address expected value signal 616 is that the address component included in the ID information of the DVD 101 has a rule that when the sector is advanced by one, the address component is also advanced by one.

Specification at page 66, line 4:

The ID information address translation block 407 takes in the current ID information signal ~~418~~417 at each ECC block synchronization signal ~~419~~418 and generates a sector address 419 and ECC block address 420 that are the base addresses of the buffer memories storing the sector and ECC block, respectively. Here, the sector address 419 must be set to include 26 or more regions for storing the frames, and the ECC block address 420 must be set to include 16 or more regions for storing the sectors.

Specification at page 66, line 13:

Lastly, an eventual generation of a data storage address in the buffer memory 106 will be described with reference to Figure 2. Figure 2 shows a

structure of address generation means 1202 of this embodiment. In Figure 2, reference numeral 201 denotes a byte counter, reference numeral 202 denotes a frame synchronization counter value address translation decoder, reference numeral 203 denotes a low order ID address translation decoder, reference numeral 204 denotes an adder/subtracter, reference numeral 205 denotes a high order ID address translation decoder, and reference numeral 206 denotes an adder. In this regard, the frame synchronization counter value address translation block 311 in Figure 3 is equivalent to the frame synchronization counter value address translation decoder 202 in Figure 2, and the ID information address translation block 407 in Figure 4 is constituted by the low order ID address translation decoder 203, adder/subtracter 204, and high order ID address translation decoder 204205.

Specification at page 67, line 16:

The frame synchronization counter value address translation decoder 202 is a decoder that takes in the absolute frame position signal 327 at the frame synchronization signal 323 and provides an output shown in Figure 9(a) with respect to the input of the absolute frame position signal 327, and the decoding result is output as the frame address 332 to the adder 205206.

Specification at page 67, line 23:

The low order ID address translation decoder 203 is a decoder that takes in the low order four bits of the current ID information signal 417 at the sector synchronization signal 331 and provides an output shown in Figure 9(b) with respect to the input of the low order four bits of the current ID information signal 417, and the decoding result is output as the sector address 419 to the adder 205206.

Specification at page 68, line 6:

The adder/subtracter 204 subtracts the high order 20 bits of the ID information 221 corresponding to the data that is preset by the control microcomputer 108 and requested from the host 109 from the high order 20 bits of the current ID information signal 417. In this process, the respective low order

four bits thereof are rounded down. Positional information 212 on a start of storage into the buffer memory 106 is added to the calculation result, and the result thereof is output as ECC block position information 214 to the high order ID address translation decoder ~~204~~205.

Specification at page 69, line 20:

As described above, even if the data read from the DVD 101 cannot be stored in the buffer memory 106, the address of the data storage into the buffer memory 106 is corrected to be normal by detecting an absolute position of the data in each of the data structures by means of the frame position detection block 308, frame position reliability determination block 310, and ID reliability determination block 405, and translating it into an address by means of the frame synchronization counter value address translation decoder 202, low order ID address translation decoder 203, and high order ID address translation decoder ~~204~~205, and accordingly, an optical disk drive with an enhanced replaying capability can be constructed.

Specification at page 73, line 20:

As a result, the physical ID retaining register B 1102 stores therein only the physical ID that is reliably free of error, and only the physical ID signal 1114 of the physical ID that is reliably free of error is output to the incrementer A 1103. In addition, the ID retaining register 1105 stores therein only the address component of the ID information that is reliably free of error, and only the ID signal 1117 that is reliably free of error is output to the incrementer B 1106.

Specification at page 75, line 14:

With such a configuration, in replay of a disk having data written thereon according to a defect sector management method for a DVD-RAM of skipping only a defective sector as shown in Figure 10(a) or a disk having data written thereon according to a defect sector management method for a DVD-RAM of skipping an ECC block including a defective sector as shown in Figure 10(b), the presence of a defective sector, the start address of the defective sector, and the number of defective sectors can be detected when the condition that the subtracter

1104 does not exhibit zero is satisfied and the comparator 1107 indicates the
continuity of the ID information.

Specification at page 78, line 20:

In addition, the frame synchronization code encoding block 3030 of this
embodiment is an example of the frame synchronization code readout means of
the present invention, the frame synchronization code encoding register A 501 and
frame synchronization code encoding register B 502 of this embodiment are an
example of the storage means of the present invention, the frame position
detection decoder 503 of this embodiment is an example of the continuity
determination means of the present invention, the frame synchronization code
arrangement OK counter 505 of this embodiment is an example of the counter
means of the present invention, the frame position detection result adoption
determination circuit 506 of this embodiment is an example of the frame position
determination means of the present invention, the frame position determination
condition 513 of this embodiment is an example of the predetermined condition of
the present invention, the frame synchronization counter block 307 of this
embodiment is an example of the frame position interpolation means of the present
invention, and the frame synchronization counter value address translation block
332 of this embodiment is an example of the address generation means of the
present invention.

CLAIMS:

1   7. (As Amended) The buffer memory address translation device according
2   to claim 4, characterized in that said predetermined criterion is a criterion of
3   reliability required by external control means, and

4   said sector address information selection means selects one of them the two
5   pieces of the sector address information by analyzing the criterion of reliability
6   required by said external control means and said determination result of said sector
7   address information reliability determination means.

1   9. (As Amended) A sector address information reliability determination
2   device, characterized in that the sector address information reliability

3   determination device comprises:

4   error detection means of detecting an error of sector address information
5   included in data read from an optical disk medium and having an error detection
6   code added thereto;

7   sector address information continuity determination means of comparing
8   said sector address information currently extracted from said read data with said
9   sector address information previously extracted to determine the continuity of said
10   sector address information; and

11   reliability determination means of determining the reliability of said sector
12   address information based on the result of the error detection for said sector
13   address information and the result of the continuity determination for said sector
14   address information with reference to a predetermined condition set by ~~said~~ an
15   external control means.

1   10. (As Amended) In readout from a rewritable optical disk medium
2   storing sector physical address information that is a physical address of ~~said~~ a
3   sector besides sector logical address information included in data,

4   a defective sector determination device, characterized in that the defective
5   sector determination device comprises:

6   continuity detection means of detecting a position where a difference
7   occurs between the continuity of said sector physical address information and the
8   continuity of said sector logical address information;

9   defective sector detection means of finding a defective sector using said
10   detected difference; and

11   informing means of informing an external control means of said detected
12   defective sector.